Low Noise Amplifier (LNA) Design Suitable for 2.4 GHz Radar Applications

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Abstract——**In radar systems and WLAN applications, receiver and transmitter circuits are used for information exchange and LNA (Low noise amplifier) circuits are used to ease the detection of the signal transmitted from the radar. To reduce the power consumption of LNA circuits, a more efficient, lower noise circuit design is required, but in which the gain is at the forefront while reducing the Noise Figure (NF). While the design provides these, attention should also be paid to parameters such as significant gain, dynamic range, stability and return loss. In this study, an LNA design that can be used in accordance with the Doppler radar operating principle, in which the consumed power is reduced, the gain is significantly high, and the noise is reduced to tolerable levels has been made. The designed LNA circuit has a structure that can also be used in WLAN applications. At operating frequency, NF and gain obtained 1.014 dB and 19.85 dB, respectively. By using a 2V 10mA biasing model in DC power, the operation of the active elements is ensured.**

Keywords—LNA, doppler radar, noise figure, impedance matching, series feedback

I. INTRODUCTION

Low-noise amplifiers are used as a key element for amplifying low-level signals at the inputs of many communication systems [1]–[3]. Low-noise amplifiers are important and widely used elements in the receiver and transmitter circuits of radar systems, WLAN applications, mobile radio systems [4], [5]. In such applications, low-noise amplifiers determine the dynamic range because they act on a certain frequency or frequency band [6], [7].

Low-noise amplifiers in receiver and transmitter circuits, which are encountered in applications such as radar, WLAN, mobile radio systems, are the circuit units in which the low amplitude signals coming from the receiving antennas are processed first, to speak on behalf of the receiver circuit [3]. The low noise of the amplifier used here plays an effective role in obtaining the desired message or, more accurately, the information without distortion or with the least distortion after the incoming signal exits the amplifier. On the other hand, noise has an important place in low-noise amplifier designs, since the less the amplifier internal noise affects the information to be transmitted on behalf of the transmitter circuits, the cleaner information signal will be obtained. This noise can be caused by the active element in low-noise amplifier circuits and the effect of environmental factors such as heat. The fact that the noise factor has little effect on the signal is a sought-after feature in low-noise amplifier circuits, in the same way, the gain of the amplifier is one of the key points to be considered together with the noise [8]. The processes for reducing the noise should be optimized in such a way as to affect the amplifier gain as little as possible. These two parameters are closely related to the dynamic range and the sensitivity of the transmitter and receiver circuits as previously mentioned in this paper. Besides being low in noise factor, reducing the power dissipation while feeding the amplifier is a desired feature for low-noise amplifier design as well [1],[2],[8]. In low-noise amplifier designs, it is aimed to increase the signal level by the amplifier gain, but while this signal is amplified, the DC power to be consumed for the active element must be reduced. In addition to these parameters, appropriate impedance values should be selected by analyzing at the stability circles of transistor to prevent the active element from oscillating. The oscillation state must be considered when optimizing the return loss values of the low-noise amplifier circuit.

Doppler radar circuits are a type of radar that uses the Doppler effect in receiving the echo signal. The purpose of Doppler radars is to distinguish between moving and non-moving objects, and if they are moving, to detect their speed [9]. In radar systems, low-noise amplifier circuits are used to amplify the signal level.

In this study, two-stage low-noise amplifier design, which is in the initial stages of radar transceiver circuits, in which the speed of motion can be detected by Doppler effect, was made using micro-strip transmission lines. Simulation was carried out by paying attention to parameters such as gain, noise factor, dissipated power, stability, return loss in a doppler radar circuit with a frequency of 2.4 GHz. The values obtained because of the simulation highly meet the targets determined before the simulation. A two-stage circuit was used to increase the gain, and serial feedback technique was used to reduce the noise factor, and values were obtained showing that it was suitable for our design goals by simulation. As a result of the simulation of the circuit, gain 19.85 dB, NF 1.014 dB, return loss as -10.02 dB for input and -19.7 dB for output obtained at 2.4 GHz frequency.

II. LOW NOISE AMPLIFIER DESIGN

A. *Structure of the Amplifier*

The elements and topologies of the proposed low-noise amplifier circuit consist of the input matching circuit, transistors as our active elements, transistor serial feedbacks, and output matching circuit. The low-noise amplifier topology is shown in Figure 1. Microstrip transmission lines are used in the design of low-noise amplifier circuit elements modeled in Figure 1. Low-noise amplifier design was carried out by using FR4 material simulation parameters as the substrate surface in the microstrip transmission line. FR4 was preferred due to cost and ease of access.

The DC supply part of the transistor shown in Figure 1 is simulated using the 2V 10mA linear model [10]. Transistor selection was made by considering its stability, gain at effective frequency, noise factor, and return loss as well as DC supply. Input and output matching circuits were also designed with microstrip transmission lines by determining the optimization goals of noise, gain, return loss parameters. The block diagram of the designed low-noise amplifier circuit is shown in Figure 2.

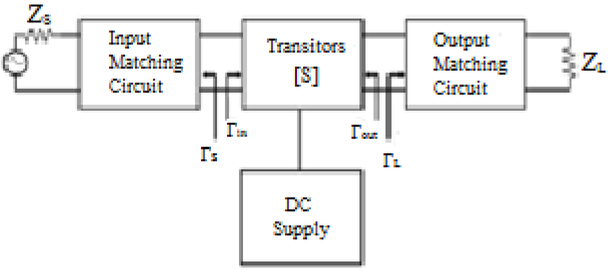

Fig. 1. Low Noise Amplifier(LNA) topology

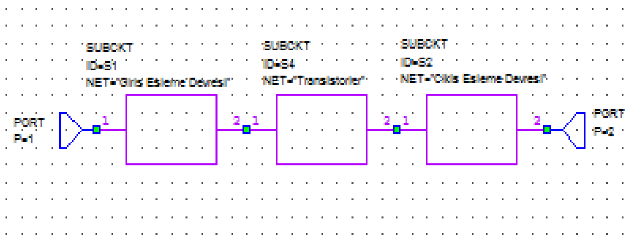

Fig. 2. Designed low noise amplifier(LNA) block diagram

While designing the circuit whose block diagram is shown in Figure 2, the optimization parameters of the transmission lines and the desired values of these parameters in the design were determined. In line with these goals set out in Table 1, adjustments were made on the transmission lines through the optimize tool of the Cadence AWR DE (Design Environment) MWO (Microwave Office) program. The goals determined in Table 1 were optimized in the 1-6GHz range to include the operating frequency.

TABLE I. OPTIMIZATION GOALS

	Noise Figure	Gain	Return Loss	
	NF	***S_{21}***	***S_{11}(Input)***	***S_{22}(Output)***
1-2GHz	-	-	<0dB	<0dB
2-3GHz	<1.5dB	>15dB	<-10dB	<-10dB
3-6GHz	-	-	<0dB	<0dB

As shown in Table 1, the noise figure (NF) is aimed to remain below 1.5 dB in the 2-3 GHz range, which includes the operating frequency, and its effect on the signal is reduced. Here, while calculating the noise figure in the simulation, operations were carried out based on the following formulas. In the following equations 1, 2, 3 and 4, SNR_o is the signal-to-noise ratio at the output, SNR_i is the signal-to-noise ratio at the input, A is the gain of the designed amplifier, P_s is the signal power, P_N is the noise power, P_{ND} is the power of its own noise, F is the actual value of the noise.

$$SNR_o = \frac{A \times P_S}{A \times (P_N + P_{ND})} \tag{1}$$

$$SNR_i = \frac{P_S}{P_N} \tag{2}$$

$$F = \frac{SNR_i}{SNR_o} \tag{3}$$

$$NF = 10\,log_{10}(F) = 10\,log_{10}\left(\frac{SNR_i}{SNR_o}\right) \tag{4}$$

Similarly, the gain parameter of the low-noise amplifier in Table 1, S_{21}, was optimized with transmission lines to be above 15 dB to obtain a high gain. The lengths and widths of the transmission lines were optimized using the following formulas and with the AWR MWO optimizer tool in line with the optimization goals. W, d specified in equation 5, represents the width of the transmission lines and the thickness, respectively. $\mathcal{E}_r$ is the dielectric constant and $\mathcal{E}_{r,eff}$ is the effective value of it. The impedance Z_o is 50 Ω.

$$\frac{W}{d} = \begin{cases} \frac{8e^A}{e^{2A}-2} & , \frac{W}{d} < 2 \\ \frac{2}{\pi}\left[B - 1 - \ln(2B-1) + \frac{\varepsilon_r - 1}{2\varepsilon_r}\left(\ln(B-1) + 0.39 - \frac{0.61}{\varepsilon_r}\right)\right] & , \frac{W}{d} > 2 \end{cases} \tag{5}$$

$$A = \frac{Z_0}{60}\sqrt{\frac{\varepsilon_r+1}{2}} + \frac{\varepsilon_r-1}{\varepsilon_r+1}\left(0.23 + \frac{0.11}{\varepsilon_r}\right) \tag{6}$$

$$B = \frac{377\pi}{2Z_0\sqrt{\varepsilon_r}} \tag{7}$$

$$\lambda = \frac{c}{f\sqrt{\varepsilon_{r,eff}}} \tag{8}$$

$$\varepsilon_{r,eff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\frac{1}{\sqrt{1+12\frac{d}{W}}} \tag{9}$$

In the two-port low-noise amplifier circuit, there are two parameters for the return loss evaluation, S_{11} for the input part and S_{22} for the output part. In the 2-3 GHz band, which is the range of the operating frequency, it is determined as a goal for these two parameters to be below -10 dB. The goal of wanting these two parameters to be low is to have low reflection in the range where our amplifier circuit operates. To design a more efficient circuit, reducing the reflection is the key point of it. In the remaining parts of the test frequency range, 1-2 GHz and 3-6 GHz, the values of S_{11} and S_{22} are intended to be below 0 dB so that the transistor does not oscillate. As in S_{21}, the goals were achieved by adjusting the length and width with the above equations.

B. Designing the Part of the Amplifier

While designing, first, the transistors in the transistor block of the LNA circuit, which was created by drawing the block diagram in Figure 2 in the previous section, and the feedback of the transistors were designed in simulation. Selected ATF-55143 model GaAs FET transistors specified S1 and S2, as seen in Figure 5, a two-stage circuit was created to increase the gain by connecting the drain end of S1 transistor to the gate end of S2 transistor.

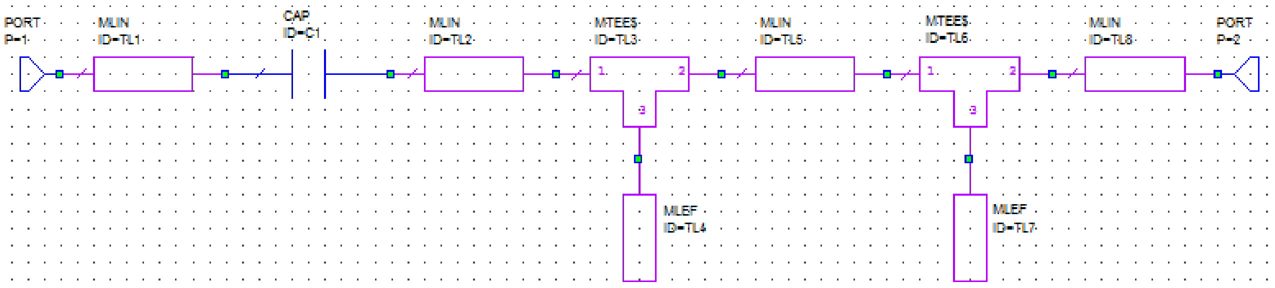

Fig. 3. Input matching circuit schematic

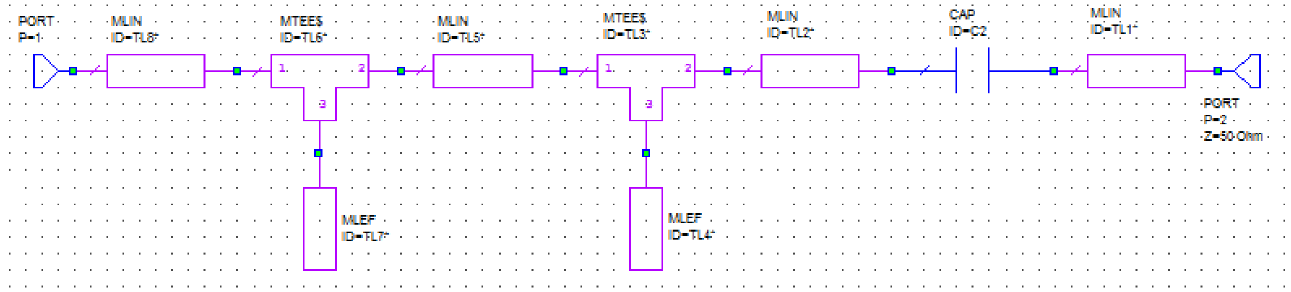

Fig. 4. Output matching circuit schematic

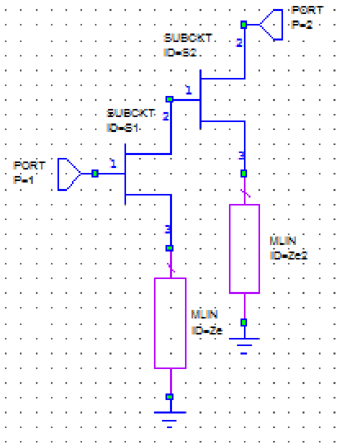

Fig. 5. Transistor circuit schematic

In order to facilitate the optimization of the NF value and reduce the NF, the transmission lines expressed as Z_e and Z_{e2} in the schematic in Figure 5 are fed back to the transistors in series [3], [10].

Following the transistor schematic, suitable input and output matching circuits were designed through optimization of the transmission lines. While designing the input and output matching circuits, the transmission lines specified in Figure 3 and Figure 4 as TL1 and TL1* are set 50 Ω by adjusting their width and length at 2.4GHz using the TXLine tool of the AWR MWO program, to first comply with the port impedance and thus avoid any loss when it comes to the real time application of the designed circuit. Capacitors specified as C1 in the input matching circuit and C2 in the output matching circuit were used to prevent the DC supply voltage from escaping to the ports when the real application of the circuit is made in the future. To provide the optimization parameters specified in Table 1 of the input and output matching circuits in Figure 3 and Figure 4, the part from TL2 and TL2* transmission lines to TL8 and TL8* transmission lines was designed as pi matching circuit [11]. Transmission lines specified as TL4, TL4*, TL7, TL7* in the pi matching section were designed with open circuit termination. As seen in Figures 3 and 4, the pi matching circuit facilitates the optimization by ensuring that the transmission line specified by TL3 is properly connected with the first port TL2, the second port TL5 and the third port TL4. Like the TL3 transmission line, the TL6 transmission line also provides the appropriate connection by connecting to its ports TL5, TL8, TL7 respectively. TL3* and TL5* transmission lines, which perform the same operation in the output matching circuit in Figure 5, are designed as their counterparts in the input matching circuit.

III. SIMULATION RESULTS AND DISCUSSION

The structures proposed in Figure 2 for the low-noise amplifier circuit are combined into a single topology. NF, gain and return loss measurements were made in the AWR MWO environment. In Figure 6, the NF graph of the LNA circuit designed with transmission lines is obtained because of simulation at 1-6 GHz frequency range. As indicated in the graph in Figure 6, NF is seen as 1.014 dB at 2.4 GHz operating frequency. It complies with the optimization goals set for noise before the design.

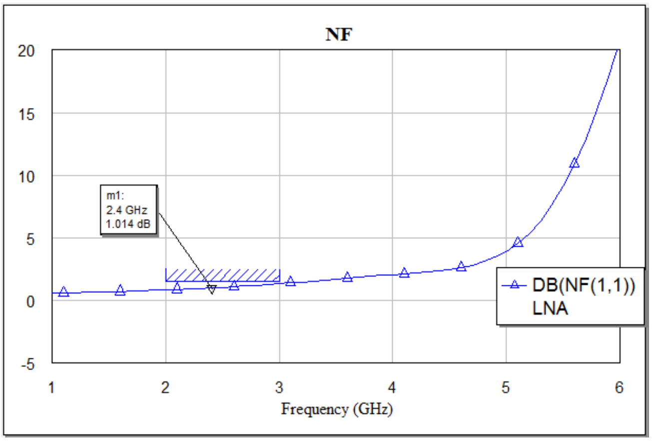

Fig. 6. NF graph of the designed circuit between 1-6 GHz

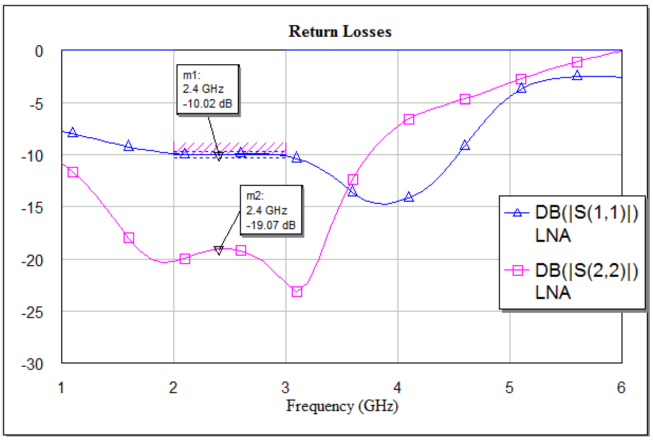

Fig. 7. Return loss graph of the designed circuit between 1-6 GHz

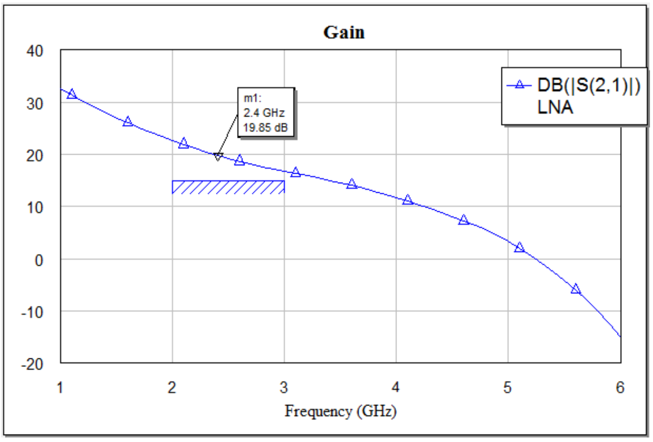

Fig. 8. Gain graph of the designed circuit between 1-6 GHz

The graph of the return loss values of the designed circuit, S_{11} and S_{22}, between 1-6 GHz was obtained as seen in Figure 7. The S_{11} and S_{22} values determined for optimization and required to be below -10 dB in the design are seen as -10.02 dB and -19.07 dB, respectively, in accordance with the goal. The gain graph of the proposed LNA circuit is shown in Figure 8 at 1-6 GHz frequency range at 2.4 GHz, a gain of 19.85 dB is provided in accordance with the goals. The gain obtained due to the design appears suitable for the intended use of the circuit.

Operating frequency band can be adjusted to appeal to different usage purposes. By using recent developments in technology, the gain can be increased, and the power consumed can be reduced. As a result, the values obtained by simulation in this study were obtained in coherent with the purpose and objectives.

IV. CONCLUSION

In this study, we designed the LNA circuit using transmission lines for doppler radar applications operating at 2.4 GHz frequency and simulated it using AWR MWO. We used FR4 material for transmission lines due to its low cost and ease of access. We used AWR MWO program, AWR MWO optimize and TXLine tools for optimization, simulation, and analysis. The analysis results of the proposed LNA circuit are shown in Figure 6, Figure 7 and Figure 8. The analysis results shown that the design is suitable for the goals determined before the design. At 2.4 GHz, the NF remains below 1.5 dB and is seen as 1.014 dB. Return loss values for the same frequency are below -10 dB and S_{11} is -10.02 dB and S_{22} -19.07 dB. The gain is seen as 19.85 dB at a value higher than 15 dB.

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